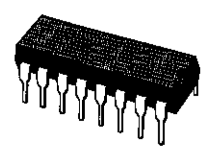
# HCC40105B
# HCF40105B

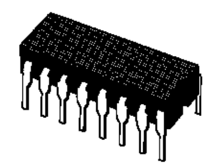
SGS-THOMSON MICROELECTRONICS

## FIFO REGISTER

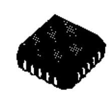
- INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS
- 3-STATE OUTPUTS
- EXPANDABLE IN EITHER DIRECTION
- STATUS INDICATORS ON INPUT AND OUTPUT
- RESET CAPABILITY
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



**EY**
(Plastic Package)



**F**
(Ceramic Package)



**C1**
(Chip Carrier)

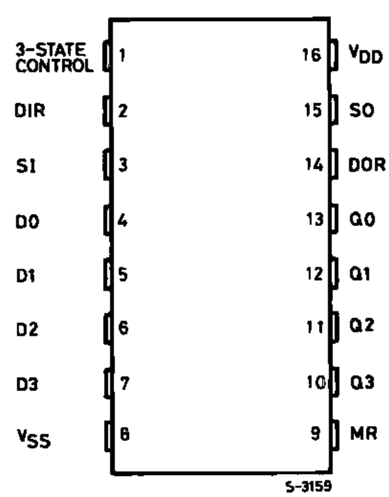
**ORDER CODES :**
HCC40105BF HCF40105BEY
HCF40105BC1

### DESCRIPTION

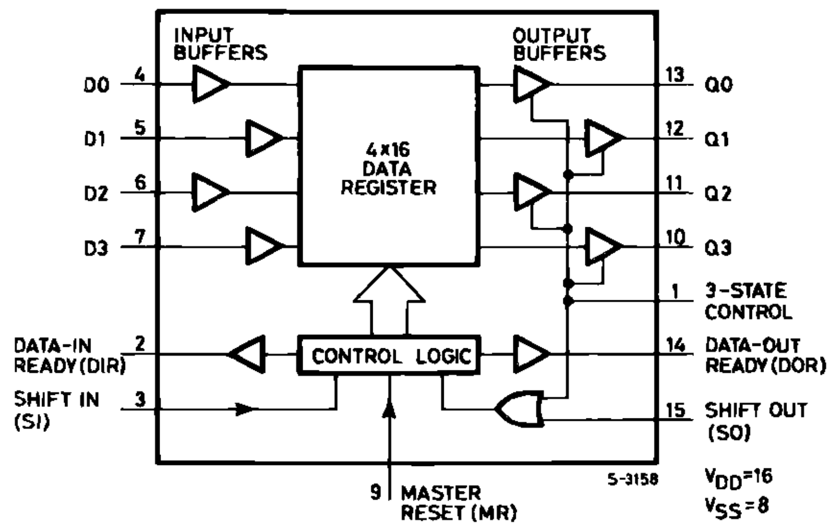
The **HCC40105B** (extended temperature range) and **HCF40105B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **HCC/HCF40105B** is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

**PIN CONNECTIONS**



## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

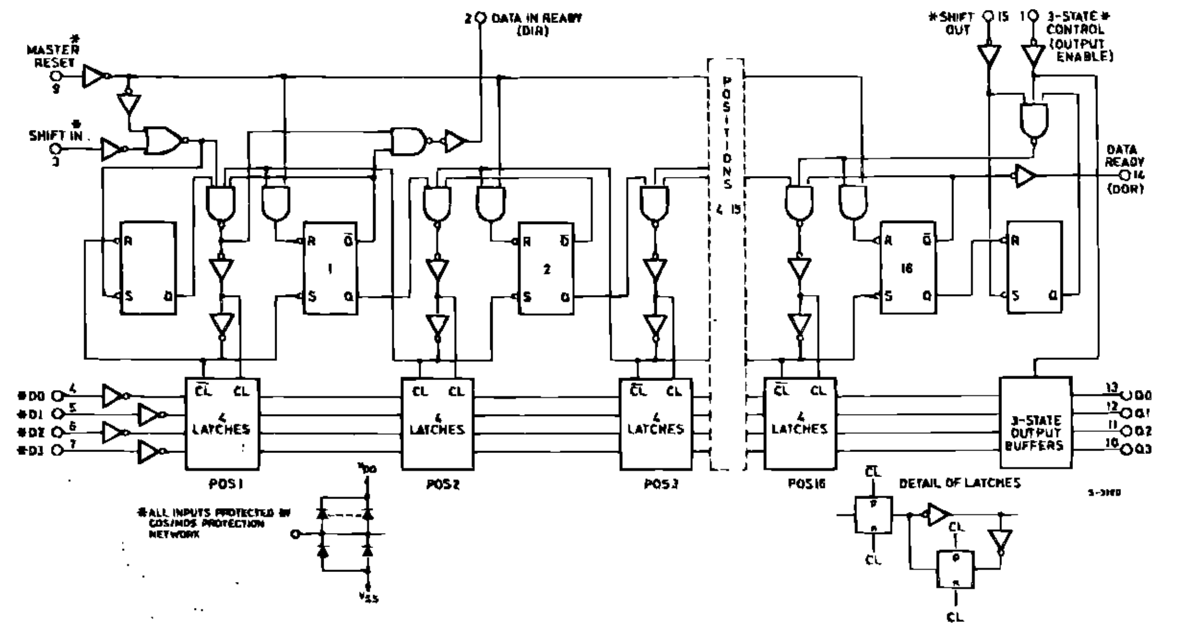
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$* | Supply Voltage : **HCC** Types<br>**HCF** Types | – 0.5 to + 20<br>– 0.5 to + 18 | V<br>V |
| $V_i$ | Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_I$ | DC Input Current (any one input) | ± 10 | mA |
| $P_{tot}$ | Total Power Dissipation (per package)<br>Dissipation per Output Transistor<br>for $T_{op}$ = Full Package-temperature Range | 200<br><br>100 | mW<br><br>mW |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to $V_{SS}$ pin voltage.

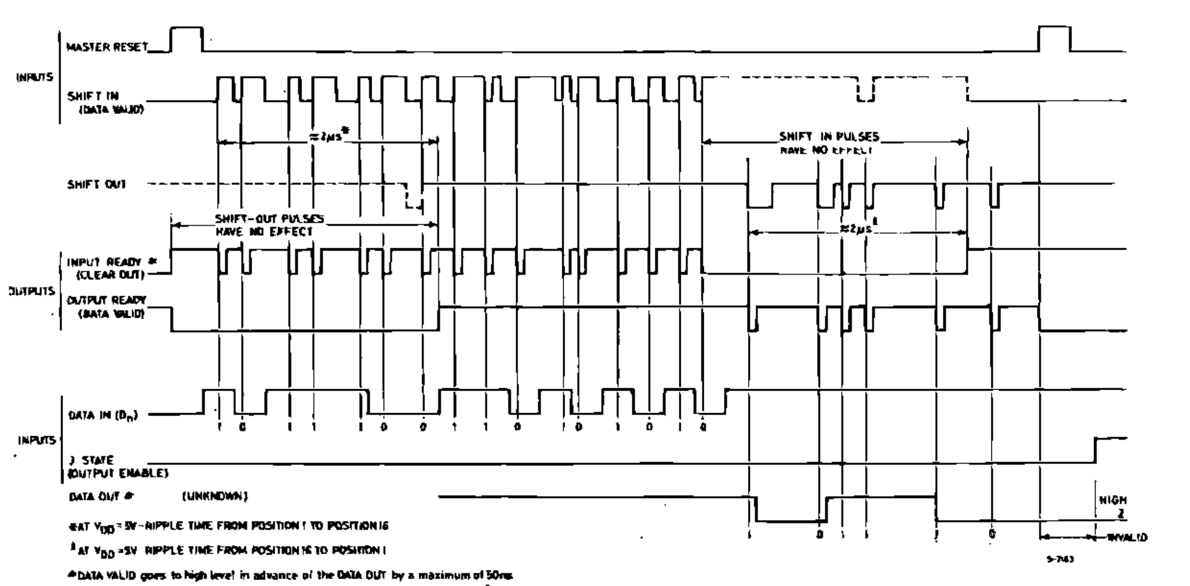
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage : **HCC** Types<br>**HCF** Types | 3 to 18<br>3 to 15 | V<br>V |
| $V_I$ | Input Voltage | 0 to $V_{DD}$ | V |
| $T_{op}$ | Operating Temperature : **HCC** Types<br>**HCF** Types | – 55 to + 125<br>– 40 to + 85 | °C<br>°C |

## LOGIC DIAGRAM




## TIMING DIAGRAM



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

| Symbol | Parameter | | Test Conditions | | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ (V) | $V_O$ (V) | $\lvert I_O \rvert$ (μA) | $V_{DD}$ (V) | $T_{Low}$* | | 25°C | | | $T_{High}$* | | |
| | | | | | | | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $I_L$ | Quiescent Current | HCC Types | 0/ 5 | | | 5 | | 5 | | 0.04 | 5 | | 150 | μA |
| | | | 0/10 | | | 10 | | 10 | | 0.04 | 10 | | 300 | |
| | | | 0/15 | | | 15 | | 20 | | 0.04 | 20 | | 600 | |
| | | | 0/20 | | | 20 | | 100 | | 0.08 | 100 | | 3000 | |
| | | HCF Types | 0/ 5 | | | 5 | | 20 | | 0.04 | 20 | | 150 | |
| | | | 0/10 | | | 10 | | 40 | | 0.04 | 40 | | 300 | |
| | | | 0/15 | | | 15 | | 80 | | 0.04 | 80 | | 600 | |
| $V_{OH}$ | Output High Voltage | | 0/ 5 | | < 1 | 5 | 4.95 | | 4.95 | | | 4.95 | | V |
| | | | 0/10 | | < 1 | 10 | 9.95 | | 9.95 | | | 9.95 | | |
| | | | 0/15 | | < 1 | 15 | 14.95 | | 14.95 | | | 14.95 | | |
| $V_{OL}$ | Output Low Voltage | | 5/0 | | < 1 | 5 | | 0.05 | | | 0.05 | | 0.05 | V |
| | | | 10/0 | | < 1 | 10 | | 0.05 | | | 0.05 | | 0.05 | |
| | | | 15/0 | | < 1 | 15 | | 0.05 | | | 0.05 | | 0.05 | |
| $V_{IH}$ | Input High Voltage | | | 0.5/4.5 | < 1 | 5 | 3.5 | | 3.5 | | | 3.5 | | V |
| | | | | 1/9 | < 1 | 10 | 7 | | 7 | | | 7 | | |
| | | | | 1.5/13.5 | < 1 | 15 | 11 | | 11 | | | 11 | | |
| $V_{IL}$ | Input Low Voltage | | | 4.5/0.5 | < 1 | 5 | | 1.5 | | | 1.5 | | 1.5 | V |
| | | | | 9/1 | < 1 | 10 | | 3 | | | 3 | | 3 | |
| | | | | 13.5/1.5 | < 1 | 15 | | 4 | | | 4 | | 4 | |
| $I_{OH}$ | Output Drive Current | HCC Types | 0/ 5 | 2.5 | | 5 | – 2 | | – 1.6 | – 3.2 | | – 1.15 | | mA |
| | | | 0/ 5 | 4.6 | | 5 | – 0.64 | | – 0.51 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.6 | | – 1.3 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 4.2 | | – 3.4 | – 6.8 | | – 2.4 | | |
| | | HCF Types | 0/ 5 | 2.5 | | 5 | – 1.53 | | – 1.36 | – 3.2 | | – 1.1 | | |
| | | | 0/ 5 | 4.6 | | 5 | – 0.52 | | – 0.44 | – 1 | | – 0.36 | | |
| | | | 0/10 | 9.5 | | 10 | – 1.3 | | – 1.1 | – 2.6 | | – 0.9 | | |
| | | | 0/15 | 13.5 | | 15 | – 3.6 | | – 3.0 | – 6.8 | | – 2.4 | | |
| $I_{OL}$ | Output Sink Current | HCC Types | 0/ 5 | 0.4 | | 5 | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | | 0/10 | 0.5 | | 10 | 1.6 | | 1.3 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 4.2 | | 3.4 | 6.8 | | 2.4 | | |
| | | HCF Types | 0/ 5 | 0.4 | | 5 | 0.52 | | 0.44 | 1 | | 0.36 | | |
| | | | 0/10 | 0.5 | | 10 | 1.3 | | 1.1 | 2.6 | | 0.9 | | |
| | | | 0/15 | 1.5 | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| $I_{IH}$, $I_{IL}$ | Input Leakage Current | HCC Types | 0/18 | Any Input | | 18 | | ± 0.1 | | $\pm 10^{-5}$ | ± 0.1 | | ± 1 | μA |
| | | HCF Types | 0/15 | | | 15 | | ± 0.3 | | $\pm 10^{-5}$ | ± 0.3 | | ± 1 | |
| $I_{OH}$,$I_{OL}$** | 3-State Output Leakage Current | HCC Types | 0/18 | 0/18 | | 18 | | ± 0.4 | | $\pm 10^{-4}$ | ± 0.4 | | ± 12 | μA |
| | | HCF Types | 0/15 | 0/15 | | 15 | | ± 1.0 | | $\pm 10^{-4}$ | ± 1.0 | | ± 7.5 | |
| $C_I$ | Input Capacitance | | | Any Input | | | | | | 5 | 7.5 | | | pF |

* $T_{Low}$ = – 55°C for **HCC** device : – 40°C for **HCF** device.
* $T_{High}$ = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with $V_{DD}$ = 5V, 2V min. with $V_{DD}$ = 10V, 2.5 V min. with $V_{DD}$ = 15V.
* * Forced output disable.

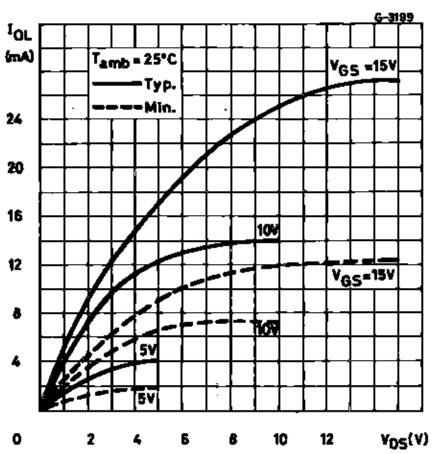
**DYNAMIC ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, $C_L$ = 50 pF, $R_L$ = 200 kΩ, typical temperature coefficient for all $V_{DD}$ values is 0.3 %/°C, all input rise and fall time = 20 ns)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{PHL}$ | Propagation Delay Time Shift-out or Reset to Data-out Ready | | 5 | | 185 | 370 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 65 | 130 | |
| $t_{PHL}$ | Propagation Delay Time Shift-in to Data-in Ready | | 5 | | 160 | 320 | ns |
| | | | 10 | | 65 | 130 | |
| | | | 15 | | 45 | 90 | |
| $t_{PZH}$, $t_{PZL}$ | Propagation Delay Time 3-state Control to Data-out | | 5 | | 140 | 280 | ns |
| | | | 10 | | 60 | 120 | |
| | | | 15 | | 40 | 80 | |
| $t_{PHZ}$, $t_{PLZ}$ | Propagation Delay Time 3-State Control to Data-out | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $t_{PLH}$ | Ripple-through Delay Input to Output | | 5 | | 2 | 4 | µs |
| | | | 10 | | 1 | 2 | |
| | | | 15 | | 0.7 | 1.4 | |
| $t_{THL}$, $t_{TLH}$ | Transition Time | | 5 | | 100 | 200 | ns |
| | | | 10 | | 50 | 100 | |
| | | | 15 | | 40 | 80 | |
| $f_I$ | Shift-in or Shift-out Rate | | 5 | | 1.5 | 3 | MHz |
| | | | 10 | | 3 | 6 | |
| | | | 15 | | 4 | 8 | |
| $t_{WH}$ | Shift-in Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 80 | 40 | | |
| | | | 15 | 60 | 30 | | |
| $t_{WL}$ | Shift-out Pulse Width | | 5 | 360 | 180 | | ns |
| | | | 10 | 160 | 80 | | |
| | | | 15 | 100 | 50 | | |
| $t_r$ | Shift-in or Shift-out Rise Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_f$ | Shift-in Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 15 | |
| | | | 15 | | | 15 | |
| $t_f$ | Shift-out Fall Time | | 5 | | | 15 | µs |
| | | | 10 | | | 5 | |
| | | | 15 | | | 5 | |
| $t_{setup}$ | Data Setup Time | | 5 | 0 | | | ns |
| | | | 10 | 0 | | | |
| | | | 15 | 0 | | | |

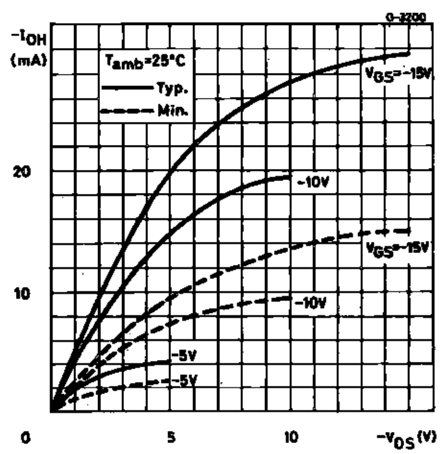
**DYNAMIC ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min. | Typ. | Max. | |
| $t_{hold}$ | Data Hold Time | | 5 | 350 | 175 | | ns |
| | | | 10 | 150 | 75 | | |
| | | | 15 | 120 | 60 | | |
| $t_{WL}$ | Data–in Ready Pulse Width | | 5 | | 260 | 520 | ns |
| | | | 10 | | 100 | 120 | |
| | | | 15 | | 70 | 140 | |
| $t_{WL}$ | Data–out Ready Pulse Width | | 5 | | 220 | 440 | ns |
| | | | 10 | | 90 | 180 | |
| | | | 15 | | 665 | 130 | |
| $t_{WH}$ | Master Reset Pulse Width | | 5 | 200 | 100 | | ns |
| | | | 10 | 90 | 45 | | |
| | | | 15 | 60 | 30 | | |

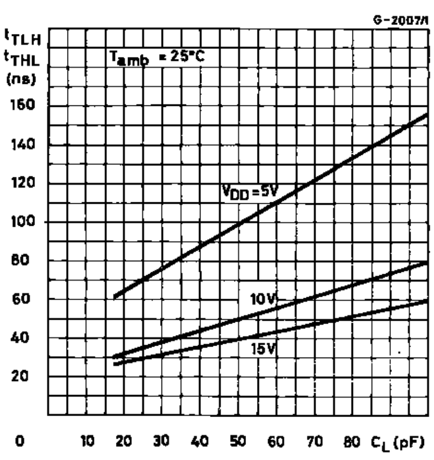
Output Low (sink) Current Characteristics.



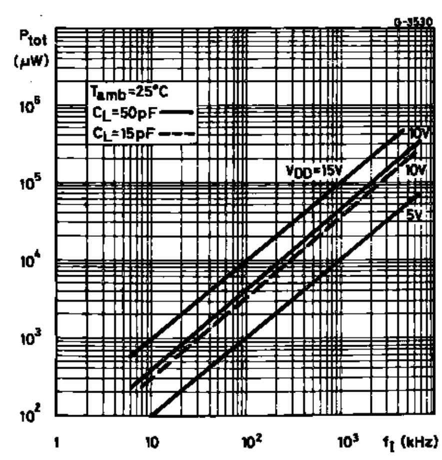

Output High (source) Current Characteristics.




Typical Transition Time vs. Load Capacitance.

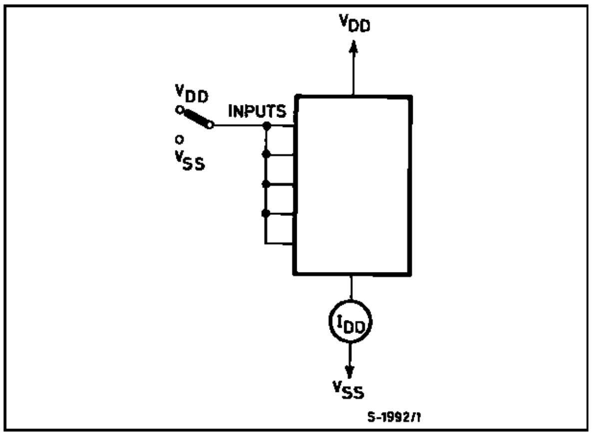



Typical Dynamic Power Dissipation vs. Frequency.

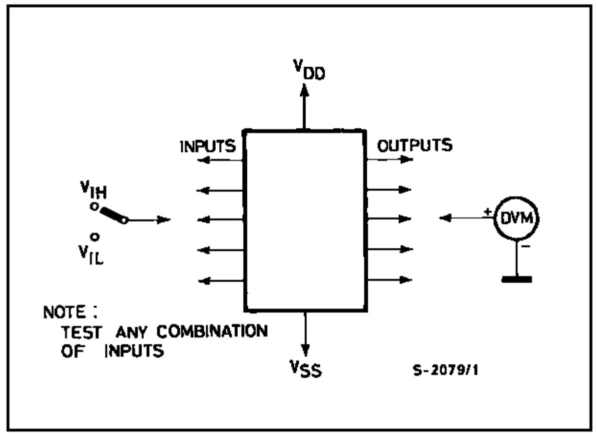


## TEST CIRCUITS

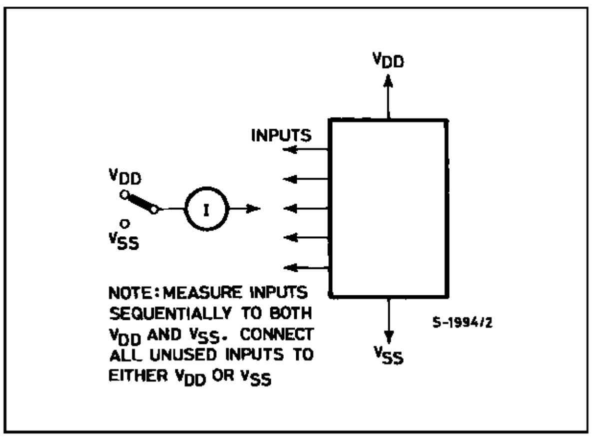
Quiescent Device Current.



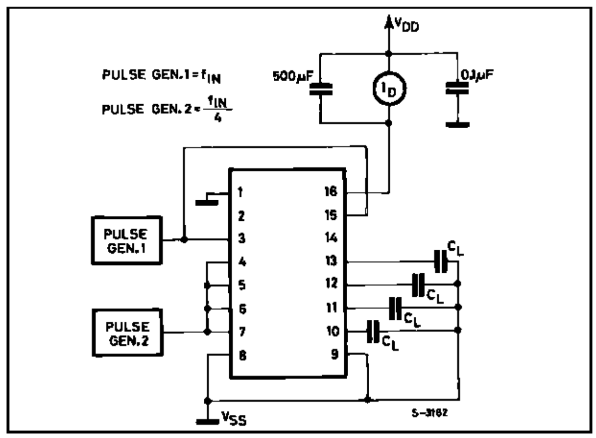

Input Voltage.




Input Leakage Current.

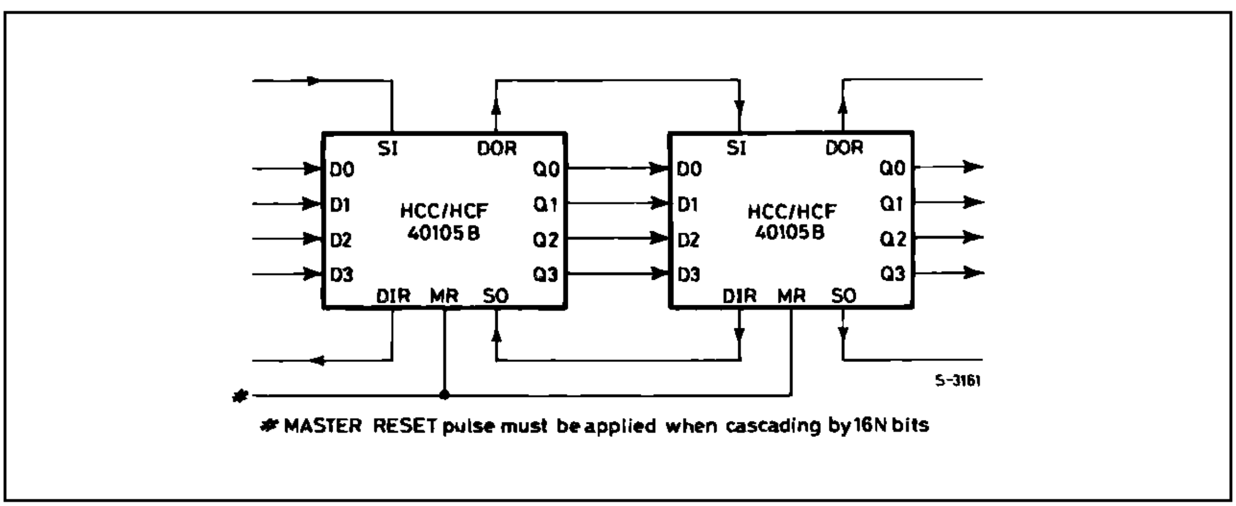



Dynamic Power Dissipation.

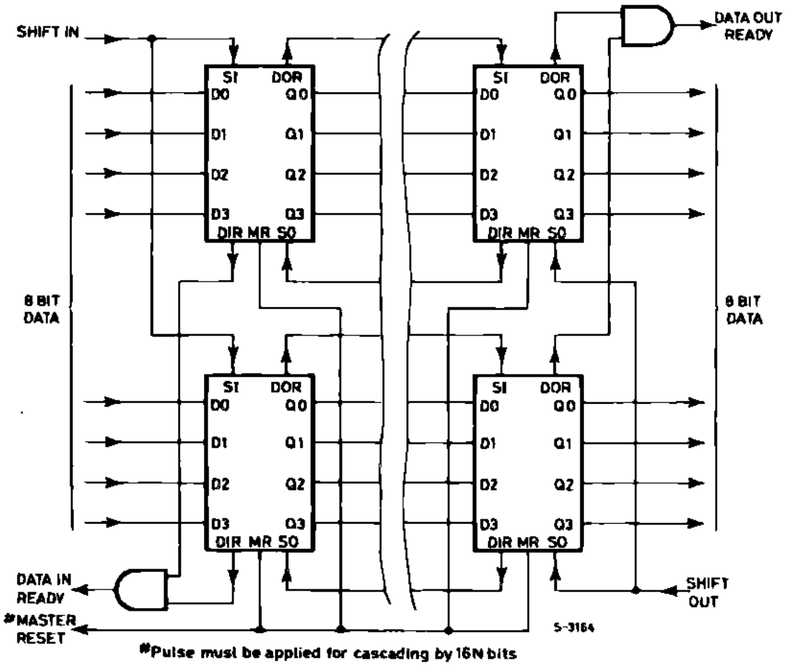



## TYPICAL APPLICATIONS

EXPANSION, 4 BITS–WIDE–BY–16 N–BITS LONG.



EXPANSION, 8 BITS–WIDE–BY–16 N–BITS LONG.




## APPLICATIONS INFORMATION

LOADING DATA

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

UNLOADING DATA

As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

CASCADING

The **HCC/HCF40105B** can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions.

3-STATE OUTPUTS

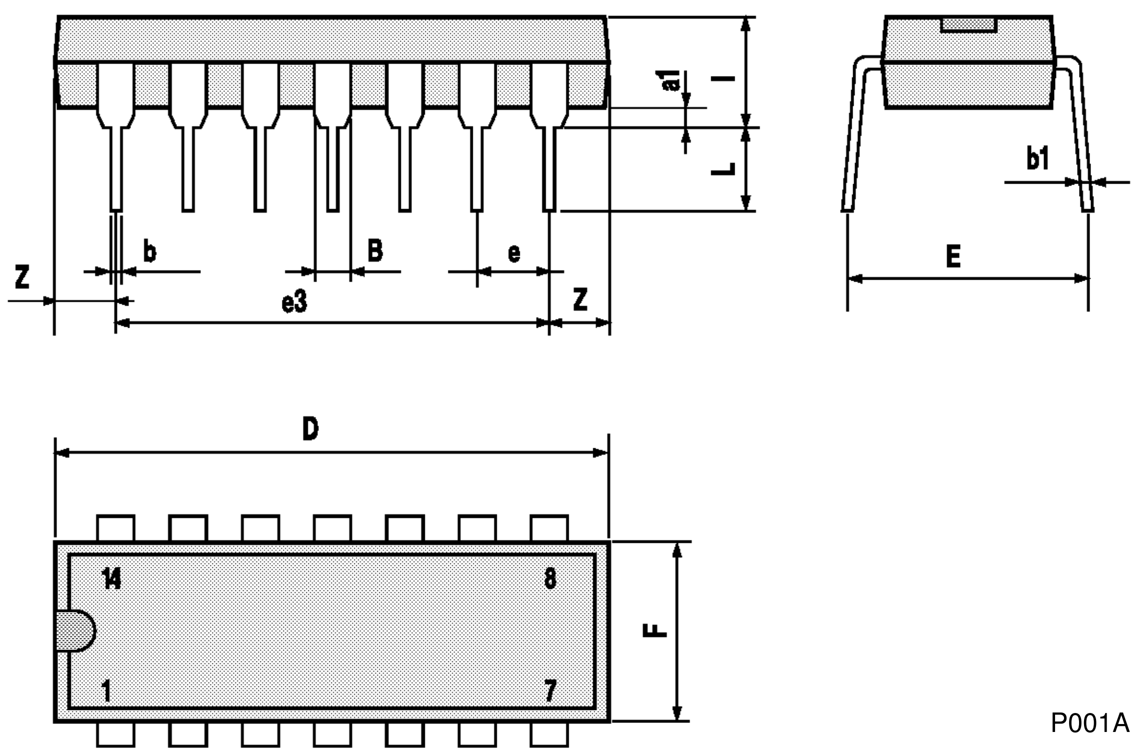
In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

MASTER RESET

A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded.

## Plastic DIP14 MECHANICAL DATA

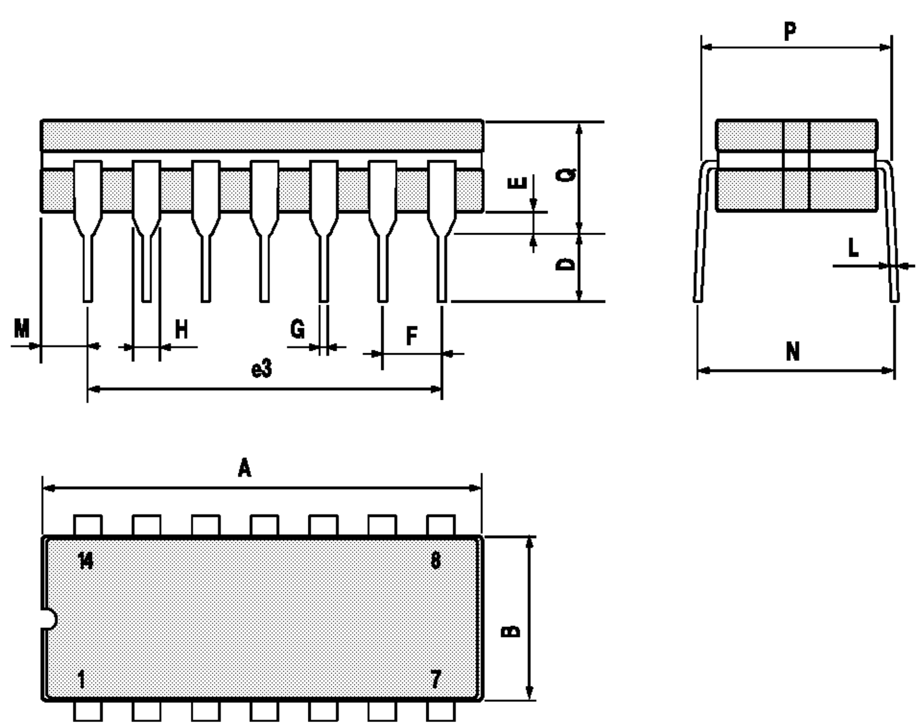
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 15.24 | | | 0.600 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | 1.27 | | 2.54 | 0.050 | | 0.100 |




P001A

## Ceramic DIP14/1 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 20 | | | 0.787 |
| B | | | 7.0 | | | 0.276 |
| D | | 3.3 | | | 0.130 | |
| E | 0.38 | | | 0.015 | | |
| e3 | | 15.24 | | | 0.600 | |
| F | 2.29 | | 2.79 | 0.090 | | 0.110 |
| G | 0.4 | | 0.55 | 0.016 | | 0.022 |
| H | 1.17 | | 1.52 | 0.046 | | 0.060 |
| L | 0.22 | | 0.31 | 0.009 | | 0.012 |
| M | 1.52 | | 2.54 | 0.060 | | 0.100 |
| N | | | 10.3 | | | 0.406 |
| P | 7.8 | | 8.05 | 0.307 | | 0.317 |
| Q | | | 5.08 | | | 0.200 |



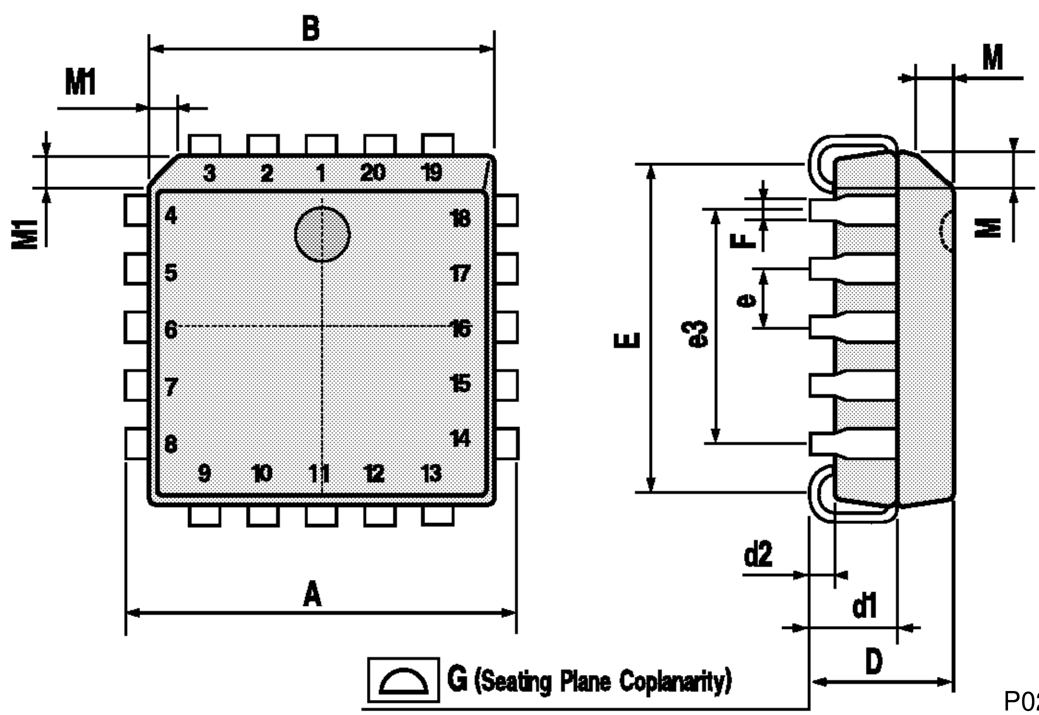

P053C



SGS-THOMSON MICROELECTRONICS

## PLCC20 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 9.78 | | 10.03 | 0.385 | | 0.395 |
| B | 8.89 | | 9.04 | 0.350 | | 0.356 |
| D | 4.2 | | 4.57 | 0.165 | | 0.180 |
| d1 | | 2.54 | | | 0.100 | |
| d2 | | 0.56 | | | 0.022 | |
| E | 7.37 | | 8.38 | 0.290 | | 0.330 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 5.08 | | | 0.200 | |
| F | | 0.38 | | | 0.015 | |
| G | | | 0.101 | | | 0.004 |
| M | | 1.27 | | | 0.050 | |
| M1 | | 1.14 | | | 0.045 | |




P027A