

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT137

**3-to-8 line decoder/demultiplexer
with address latches; inverting**

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT137

FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A_n). The "137" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the "137" acts as a 3-to-8 active LOW decoder. When the latch enable ($\overline{LE}$) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable input ($\overline{E}_1$ and E₂) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E₂ is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay A _n to $\overline{Y}_n$ $\overline{LE}$ to $\overline{Y}_n$ $\overline{E}_1$ to $\overline{Y}_n$ E ₂ to $\overline{Y}_n$	C _L = 15 pF; V _{CC} = 5 V	18 17 15 15	19 21 17 15	ns ns ns ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	57	59	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A ₀ to A ₂	data inputs
4	$\overline{\text{LE}}$	latch enable input (active LOW)
5	$\overline{\text{E}}_1$	data enable input (active LOW)
6	E ₂	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{\text{Y}}_0$ to $\overline{\text{Y}}_7$	multiplexer outputs
16	V _{CC}	positive supply voltage

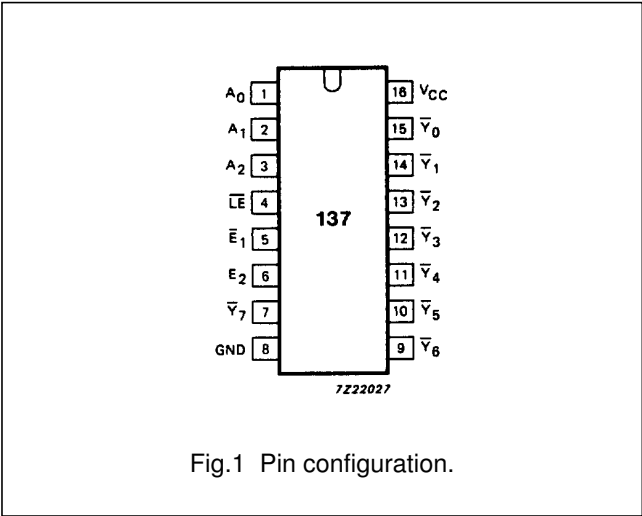


Fig.1 Pin configuration.

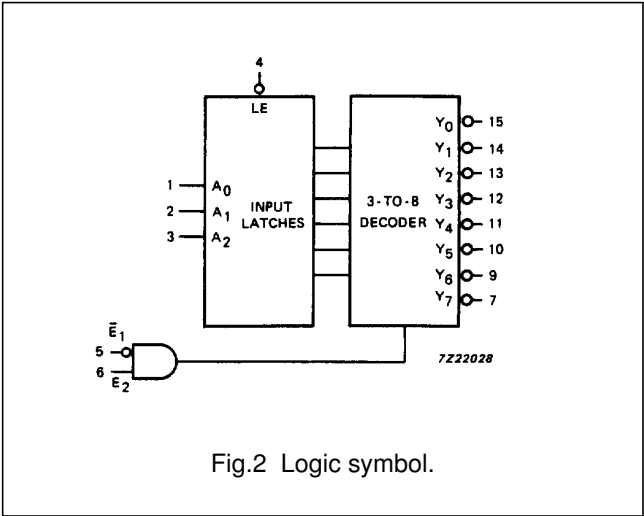


Fig.2 Logic symbol.

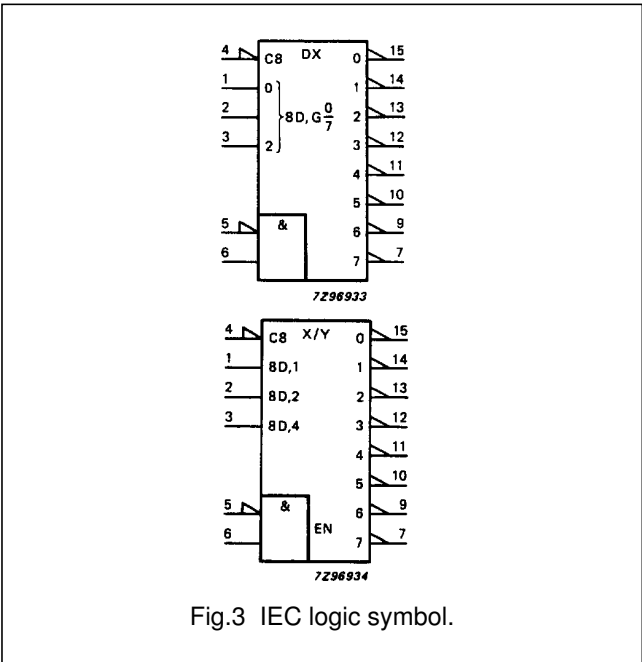


Fig.3 IEC logic symbol.

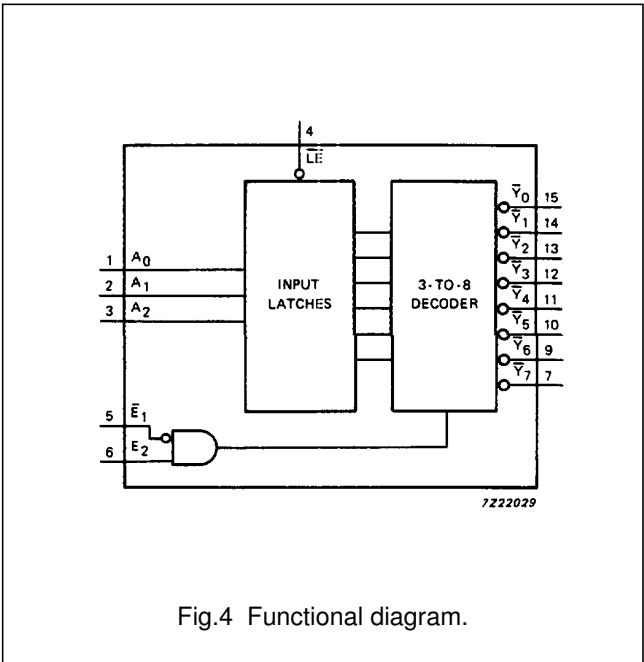


Fig.4 Functional diagram.

3-to-8 line decoder/demultiplexer with address latches; inverting

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FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care

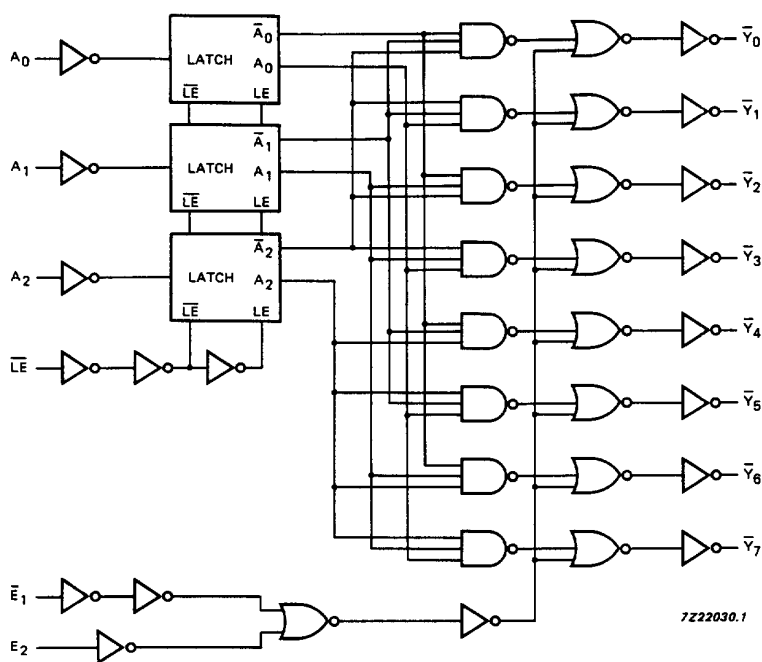


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to $\bar{Y}_n$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay $\overline{LE}$ to $\bar{Y}_n$		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay $\bar{E}_1$ to $\bar{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay E ₂ to $\bar{Y}_n$		50 18 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t _w	$\overline{LE}$ pulse width HIGH	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time A _n to $\overline{LE}$	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
t _h	hold time A _n to $\overline{LE}$	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig.8

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.50
$\overline{E}_1$	1.50
E ₂	1.50
$\overline{LE}$	1.50

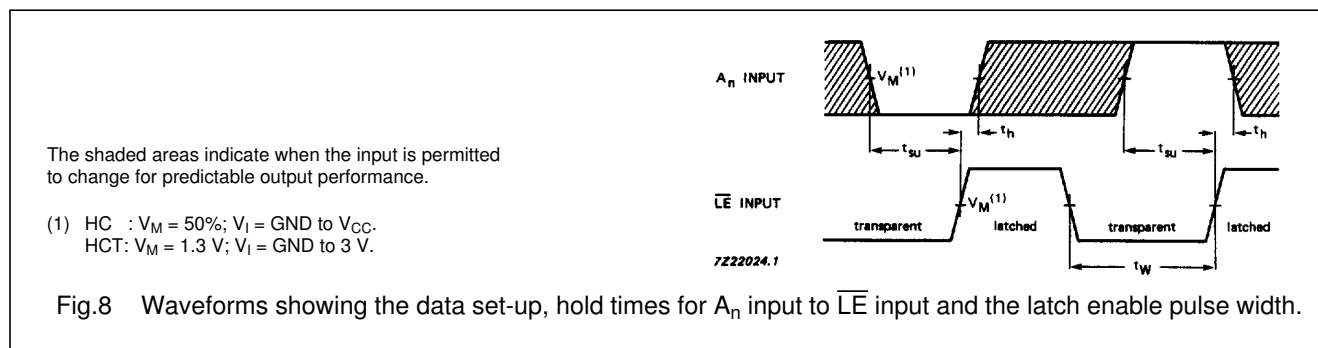
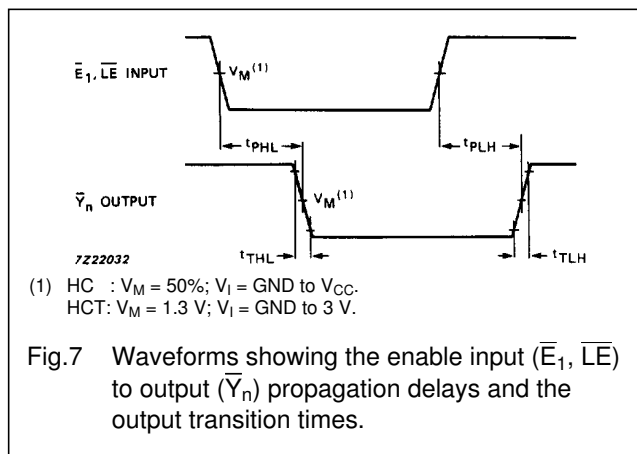
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to $\overline{Y}_n$		22	38		48		57	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay $\overline{LE}$ to $\overline{Y}_n$		25	44		55		66	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay $\overline{E}_1$ to $\overline{Y}_n$		20	37		46		56	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay E ₂ to $\overline{Y}_n$		18	35		44		53	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t _W	$\overline{LE}$ pulse width HIGH	10	5		13		15		ns	4.5	Fig.8
t _{su}	set-up time A _n to $\overline{LE}$	10	2		13		15		ns	4.5	Fig.8
t _h	hold time A _n to $\overline{LE}$	7	2		9		11		ns	4.5	Fig.8

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The diagram shows two waveforms. The top waveform, labeled A_n, E_2 INPUT, is a square wave with a high level $V_M^{(1)}$. The bottom waveform, labeled $\bar{Y}_n$ OUTPUT, is an inverted square wave. The output transitions from high to low (labeled t_{THL}) and from low to high (labeled t_{TLH}) when the input transitions from low to high. The output transitions from low to high (labeled t_{PLH}) and from high to low (labeled t_{PLH}) when the input transitions from high to low. The output transition times are labeled t_{TLH} and t_{TLH} .



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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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